Assignee: Intel Corporation

ABSTRACT OF THE DISCLOSURE

A method and apparatus for permitting out-of-order execution of predicated instructions is disclosed. In one embodiment, a predicated instruction may be decoded into a related predicated instruction and a move instruction contingent on the complementary value of the predicate of the predicated instruction. The destination register of both the related predicated instruction and the move instruction may be mapped to the same physical register, and only one of the two instructions may update machine state with its results.

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